In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Sub C1

1. (Currently Amended) A method of operating a digital system having a processor and associated translation lookaside buffer (TLB), comprising the steps of:

executing a plurality of program tasks within the processor;

initiating a plurality of memory access requests in response to the plurality of program tasks;

caching a plurality of translated memory addresses in the TLB responsive to the plurality of memory access requests;

incorporating a task identification value with each translated memory address to ~~identify~~ indicate which of the plurality of program tasks requested the respective translated memory address;

incorporating a shared indicator with each translated memory address to indicate when a translated memory address is shared by more than one of the plurality of program tasks; and

invalidating a portion of the plurality of translated memory address in the TLB in a manner that is qualified by the shared indicator in response to ~~only a single~~ an invalidate TLB entry command issued from the processor and not changing data in any other memory.

2. (Currently Amended) The method according to Claim 1, wherein:

said invalidate TLB entry command comprises an invalidate shared TLB entry command; and

the step of invalidating in response to an invalidate shared TLB entry command comprises invalidating a translated memory address in the TLB only if ~~it is~~ the corresponding shared indicator

indicates the translated memory address is shared by more than one of the plurality of program tasks.

3. (original) The method according to Claim 1, wherein:

said invalidate TLB entry command comprises an invalidate task TLB entry except shared command, said invalidate task TLB entry except shared command identifying one of the plurality of program tasks; and

the step of invalidating in response to an invalidate task TLB except shared command comprises invalidating a translated memory address in the TLB only if ~~it is~~ the corresponding task identification value indicates the program task identified by said invalidate task TLB entry except shared command and the corresponding shared indicator indicates the translated memory address is not shared by more than one of the plurality of program tasks.

4. (original) The method according to Claim 1, wherein the TLB has several levels, and wherein the step of invalidating encompasses all of the several levels of the TLB.

Claims 5 to 8. (canceled)

9. (Original) The method according Claim 1, further comprising the steps of:

maintaining a set of page translation tables for providing each translated memory address; and

including within the set of page translation tables the shared indicator for each translated memory address.

10. (Original) The method according to Claim 1, further comprising the step of maintaining a set of page translation tables

for providing each translated memory address, wherein the shared indicator for each translated memory address is not included within the set of page translation tables.

Claims 11 to 13. (Canceled)

14. (Currently Amended) A digital system having a translation lookaside buffer (TLB), the TLB comprising:

storage circuitry with a plurality of entry locations for holding translated values, wherein each of the plurality of entry locations includes a first field for a translated value and a second field for an associated shared indicator;

a set of inputs for receiving a translation request;

a set of outputs for providing a translated value selected from the plurality of entry locations; and

control circuitry connected to the storage circuitry, wherein the control circuitry is responsive to an ~~a single operation~~ invalidate TLB entry command to invalidate ~~all~~ entries ~~having a specified value in~~ within said storage circuitry qualified by the shared indicator field not change data in any other memory.

15. (Currently Amended) The digital system of Claim 14, wherein the digital system further comprises a second level TLB connected to the TLB, the second level TLB comprising:

second level storage circuitry with a plurality of entry locations for holding translated values, wherein each of the plurality of entry locations includes a first field for a translated value and a second field for an associated shared indicator; and

wherein the control circuitry is connected to the second level storage circuitry, the control circuitry being responsive to ~~the single operation~~ an invalidate TLB entry command to invalidate

selected ones of the plurality of entry locations in the second storage circuitry ~~according to~~ qualified by the shared indicator field ~~, such that qualified entry locations in the TLB and in the second level TLB are invalidated in response to the single operation command~~.

Claim 16. (Canceled)

17. (New) The digital system of Claim 14, wherein:

said invalidate TLB entry command comprises an invalidate shared TLB entry command; and

said control circuitry being responsive to an invalidate shared TLB entry command comprises to invalidate a translated memory address in the storage circuitry only if the corresponding shared indicator indicates the translated memory address is shared by more than one of the plurality of program tasks.

18. (New) The digital system of Claim 14, wherein:

said storage circuitry wherein each of the plurality of entry locations includes a third field for a task identification value;

said invalidate TLB entry command comprises an invalidate task TLB entry except shared command, said invalidate task TLB entry except shared command identifying one of a plurality of task identification values; and

control circuitry being responsive to an invalidate task TLB except shared command to invalidate a translated memory address in the storage circuitry only if the corresponding task identification value corresponds to said task identification value of said invalidate task TLB entry except shared command and the corresponding shared indicator indicates the translated memory address is not shared.